

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants: Prashant Sethi, et al.

Serial No.: 10/806,787

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For: A Method And System For Configuration
Of Processor Integrated Devices In Multi-
Processor Systems

§ Group Art Unit: 2181

§ Examiner: Chun Kuan Lee

§ Atty. Dkt. No.: ITL.1576US
§ (P18870)

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
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SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

Dear Sir:

Applicants submit the references listed on the attached form PTO 1449, copies of the non-U.S. Patent and Patent Publication references are enclosed.

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Respectfully submitted,

Date: 1/10/00

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